# Claims

[c1] 1.A fin-type field effect transistor (FinFET) comprising:
a first fin having a central channel region and source and drain regions adjacent said channel region;
a gate structure intersecting said first fin and covering said channel region; and
a second fin consisting of a channel region, said second fin being parallel to said first fin and being covered by said gate structure.

[c2] The FinFET in claim 1, wherein said second fin has a length equal to a width of said gate structure.

[c3] The FinFET in claim 1, wherein said first fin is longer than said second fin.

[c4] The FinFET in claim 1, wherein said source and drain regions of said first fin extend beyond said gate structure.

[c5] The FinFET in claim 1, wherein said second fin does not extend beyond said gate structure.

[c6] The FinFET in claim 1, further comprising source and drain contacts covering said source and drain regions of said first fin.

[c7] The FinFET in claim 1, wherein no contacts are positioned adjacent said second fin.

[c8] A fin-type field effect transistor (FinFET) comprising:
a first fin having a central channel region and source and drain regions adjacent
channel region; and
a second fin consisting of a channel region.

[c9] The FinFET in claim 8, wherein said first fin is longer than said second fin.

[c10] The FinFET in claim 8, further comprising a gate intersecting said first fin and covering said channel region.

[c11] The FinFET in claim 10, wherein said second fin has a length equal to a width of said gate structure.

[c12] The FinFET in claim 10, wherein said source and drain regions of said first fin extend beyond said gate structure.

[c13] The FinFET in claim 10, wherein said second fin does not extend beyond said gate structure.

[c14] The FinFET in claim 8, further comprising source and drain contacts covering said source and drain regions of said first fin.

[c15] The FinFETs in claim 8, wherein no contacts are positioned adjacent said second fin.

[c16] A method of manufacturing a fin-type field effect transistor (FinFET), said method comprising:

patterning a rectangular sacrificial mandrel on a hard-mask overlying a semiconductor layer;

forming sidewalls along the vertical surfaces of said mandrel;

removing said mandrel;

etching portions of said hard-mask not protected by said sidewalls;

removing said sidewalls;

etching portions of said semiconductor layer not protected by said hard-mask sidewalls to leave a freestanding rectangular loop of semiconductor material having two longer fins and two shorter sections, wherein said longer fins are perpendicular to said shorter sections;

patterning a rectangular gate conductor over central sections of said two longer fins, wherein said gate conductor intersects to said two longer fins;

doping portions of said semiconductor material not covered by said gate conductor to form source and drain regions in portions of said fins that extend beyond said gate;

forming insulating sidewalls along said gate conductor comprising a gate structure;

covering said gate conductor and said semiconductor material with a conductive contact material;

forming a contact mask over a portion of said conductive contact material that is above source and drain regions of a first fin of said two longer fins; and

selectively etching regions of said conductive contact material and said semiconductor material not protected by said contact mask,

wherein said selective etching process leaves said conductive contact material on source and drain regions of said first fin, and

wherein said selective etching process removes source and drain regions of a second fin of said two longer fins.

[c17] The FinFET in claim 16, wherein, after said selective etching process, said first fin is longer than said second fin.

[c18] The FinFET in claim 16, wherein, after said selective etching process, said second fin has a length equal to a width of said gate conductor comprising a gate structure.

[c19] The FinFET in claim 16, wherein, after said selective etching process, said source and drain regions of said first fin extend beyond said gate.

[c20] The FinFET in claim 16, wherein, after said selective etching process, said second fin does not extend beyond said gate structure.

[c21] 21.The FinFET in claim 16, wherein said selective etching process forms source and drain contacts covering said source and drain regions of said first fin.

[c22] The FinFET in claim 16, wherein, after said selective etching process, no contacts are positioned adjacent said second fin.

[c23] A method of manufacturing a fin-type field effect transistor (FinFET), said method comprising:

forming at least two parallel fins on a substrate;

patterning a gate conductor over central sections of said fins, wherein said gate conductor intersects to said fins;

covering said gate conductor and said semiconductor material with a conductive contact material;

forming a contact mask over a portion of said conductive contact material that is above source and drain regions of a first fin of said fins; and

selectively etching regions of said conductive contact material and said semiconductor material not protected by said contact mask,

wherein said selective etching process leaves said conductive contact material on source and drain regions of said first fin, and

wherein said selective etching process removes source and drain regions of a second fin of said fins.

[c24] The FinFET in claim 23, wherein, after said selective etching process, said first fin is longer than said second fin.

[c25] The FinFET in claim 23, wherein, after said selective etching process, said second fin has a length equal to a width of said

gate structure.

[c26] The FinFET in claim 23, wherein, after said selective etching process, said source and drain regions of said first fin extend beyond said gate structure.

[c27] The FinFET in claim 23, wherein, after said selective etching process, said second fin does not extend beyond said gate structure.

[c28] The FinFET in claim 23, wherein said selective etching process forms source and drain contacts covering said source and drain regions of said first fin.

[c29] The FinFET in claim 23, wherein, after said selective etching process, no contacts are positioned adjacent said second fin.